UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/053,865	01/18/2002	Mario Saggio	00-CT-320	5366

25235 7590 03/05/2004

HOGAN & HARTSON LLP
ONE TABOR CENTER, SUITE 1500
1200 SEVENTEENTH ST
DENVER, CO 80202

EXAMINER	
IM, JUNGHWA M	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 03/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/053,865	SAGGIO ET AL.	
	Examiner	Art Unit	
	Junghwa M. Im	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 November 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 6-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 13-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 13, 14 and 18 recite "an edge area of said Schottky barrier diode." The specification does not explicitly disclose what defines an edge area of the diode. In addition, the specification shows the doped regions of a second conductivity type are formed in an active area only and it shows that electrodes(metal layers) are formed at the edge of the device.

Claims 15-17 and 19-21 are dependent on the rejected base claims.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 14 and 18 are rejected under 35 U.S.C. 102(b)as being anticipated by Mori et al. (US 5101244), hereafter Mori.

Regarding clams 14 and 18, insofar as understood, Fig.1A of Mori shows a Schottky barrier diode comprising:

a substrate region (13) of a first conductive type (n^+) formed underneath a semiconductor material layer (14) of the same conductivity type (n);

a metal layer (2, 3); and

at least two doped regions (15) of a second conductive type (p) formed in the semiconductor material layer, each one of said doped regions being disposed under the metal layer and being separated from the other doped region by the portions of the semiconductor layer and said substrate region by portions of said semiconductor layer,

at least one or two of the doped regions (15) is in a center of the active area of the diode and at least one of the doped region is in an edge of the active area of the diode.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4, 6-11 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mori in view of Werner et al. (US 6184545), hereafter Werner.

Regarding claims 1, 3, 8 and 9, Fig. 1A of Mori shows a Schottky barrier diode comprising:

a substrate region (13) of a first conductive type (n^+) formed underneath a semiconductor material layer (14) of the same conductivity type (n);

a metal layer (2, 3); and

at least two doped regions (15) of a second conductive type (p) formed in the semiconductor material layer, each one of said doped regions being disposed under the metal layer and being separated from the other doped region by the portions of the semiconductor layer and said substrate region by portions of said semiconductor layer.

Fig. 1 of Mori shows most aspect of the instant invention except "the doped regions are doped to equalize the charge in the semiconductor material layer so that the electric field upon the entire volume of the semiconductor material layer is constant and equal to a critical electric field of the said semiconductor material layer." Werner discloses the doped regions are doped to equalize the charge in the semiconductor material layer so that the electric field upon the entire volume of the semiconductor material layer is constant and equal to the critical electric field of the semiconductor material (col. 1, line 64-col. 2 line 3).

Note that charges are read as mobile charge carriers which are "equalized" because the reference teaches that there are no positive carriers and no negative carriers. Werner shows the doped regions equalize charge in the semiconductor material layer through having the same doping the doped region (8) and the semiconductor material layer (col. 3, lines 62-64) and equalizing a number of foreign atoms in the doped region and the semiconductor material layer (col. 1, lines 64-66). Therefore, it would be inherent that the electric field upon the entire volume of the semiconductor material layer is constant since the charge in the semiconductor material layer is equalized. Werner shows the electric field upon the entire volume of the semiconductor material layer is equal to the critical electric field of the silicon in terms of a breakdown charge of the semiconductor (col.1, line 67-col.2, line3).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Werner into the device of Mori in order to have the doped regions doped to equalize the charge in the semiconductor material layer so that the electric field upon the entire volume of the semiconductor material layer is constant and equal to the critical electric field of the semiconductor material to correspond to a breakdown charge of the semiconductor.

Also note that the limitation of "the doped regions are doped to equalize the charge in the semiconductor material layer so that the electric field upon the entire volume of the semiconductor material layer is constant and equal to a critical electric field of the said semiconductor material layer" is an operating function of device rather than a structure of device and is not a structurally distinguishing.

Claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function. *In re Danly*, 263 F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959).

"[A]pparatus claims cover what a device is, not what a device does."(emphasis in original) Hewlett-Packard Co. v. Bausch & Lomb Inc., 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

Regarding claim 2, Mori discloses that a resistive value it doped region(15; p) is higher than a resistive value in the semiconductor region(14; n-) through having the doped region(15) having a higher impurity concentration (col. 5, lines 22-26).

Regarding claims 4 and 6, Mori fails to show heavily doped body regions. Werner teaches in Fig. 2, the doped regions comprises respective body region (8) with heavily doped body regions (10) having the same conductivity type (p) of the doped regions. It would have

been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Werner into the device of Mori in order to have a heavily doped body region in the doped region since such a heavily doped region reduced a reverse current (col.4, lines 64-68).

Regarding claim 7, Mori show substantially the entire claimed structure except that the semiconductor material comprises a resistivity value lower than five ohm-cm for a breakdown voltage higher than 200V.

However, it would have been obvious to one of ordinary skill in the art at the time of the invention made to have a recited resistivity value for a range of the specified breakdown voltage for better reliability, since it would have been held that general conditions of a claim are disclosed in the prior art by showing how to control the breakdown voltage through limiting the maximum depth of the depletion region, discovering the optimum or workable ranges involves only in routine skill in the art. *In re Aller, 105 USPQ 233.*

Regarding claims 10 and 11, Mori show substantially the entire claimed structure except "said Schottky barrier diode is operational at a voltage of 500V/600V." However, it would have been obvious to one of ordinary skill in the art at the time of the invention to have an operational voltage recited in the instant invention to accommodate a high current operation, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch,* 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 13, insofar as understood, Fig. 1A of Mori shows at least one of the doped regions (15) is in a center of the active area of the diode and at least one of the doped region is in an edge of the active area of the diode.

Claims 15, 16, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mori.

Regarding claims 15 and 19, Mori show substantially the entire claimed structure except that the semiconductor material comprises a resistively value lower than five ohm-cm for a breakdown voltage higher than 200V.

However, it would have been obvious to one of ordinary skill in the art at the time of the invention made to have a recited resistively value for a range of the specified breakdown voltage for better reliability, since it would have been held that general conditions of a claim are disclosed in the prior art by showing how to control the breakdown voltage through limiting the maximum depth of the depletion region, discovering the optimum or workable ranges involves only in routine skill in the art. *In re Aller, 105 USPQ 233.*

Regarding claims 16 and 20, Mori show substantially the entire claimed structure except "said Schottky barrier diode is operational at a voltage of 600V." However, it would have been obvious to one of ordinary skill in the art at the time of the invention to have an operational voltage recited in the instant invention to accommodate a high current operation, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch,* 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Claims 17 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mori in view of Sundaram (US 5583348).

Regarding claims 17 and 21, Mori fails to show a silicide layer over the semiconductor layer. Fig. 1 of Sundaram shows a silicide layer(41) in a Schottky diode. It would have been

obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Sundaram into the device of Mori in order to have a silicide layer over the semiconductor layer in order to reduce the process step when manufactured together with a compatible transistors (col. 1, lines 50-53).

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mori and Werner as applied to claim 1 above, and further in view of Sundaram.

Regarding claim 12, the combined teachings of Mori and Werner fail to show a silicide layer over the semiconductor layer. Fig. 1 of Sundaram shows a silicide layer(41) in a Schottky diode. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Sundaram into the device of Mori in order to have a silicide layer over the semiconductor layer in order to reduce the process step when manufactured together with a compatible transistors (col. 1, lines 50-53).

Response to Arguments

Applicant's arguments with respect to pending claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jmi

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800